CLAIMS

WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:

a temperature detector setting a level of a temperature detecting signal to a level indicating a high temperature state when detecting that a chip temperature shifts from low to high and is higher than a first boundary temperature, and setting the level of the temperature detecting signal to a level indicating a low temperature state when detecting that the chip temperature shifts from high to low and is lower than a second boundary temperature that is different from the first boundary temperature; and

a control circuit changing its own operating state according to the level of the temperature detecting signal.

2. The semiconductor integrated circuit according to claim 1, wherein

said temperature detecting circuit maintains the level of the temperature detecting signal while the chip temperature is between the first boundary temperature and the second boundary temperature.

3. The semiconductor integrated circuit according to claim 2, wherein said temperature detector further comprises:

a temperature detecting unit having a resistor and a bipolar transistor, and generating a detection voltage corresponding to the chip temperature from a connecting node of the resistor and the bipolar transistor that are connected in series between a power supply line and a ground line;

a first differential amplifier comparing a first reference voltage corresponding to the first boundary temperature with the detection voltage;

a second differential amplifier comparing a second reference voltage corresponding to the second boundary temperature with the detection voltage; and

a flipflop generating the level of the temperature detecting signal according to results of the comparisons from said first and second differential amplifiers.

4. The semiconductor integrated circuit according to claim 2, wherein said temperature detecting circuit further comprises:

a temperature detecting unit having a resistor and a bipolar transistor, and generating a detection voltage corresponding to the chip temperature from a connecting node of the resistor and the bipolar transistor that are connected in series between a power supply line and a ground line;

a basic differential amplifier comparing a basic reference voltage with the detection voltage to output a result of the comparison as a basic detection voltage;

a first differential amplifier comparing a first reference voltage corresponding to the first boundary temperature with the basic detection voltage;

a second differential amplifier comparing a second reference voltage corresponding to the second boundary temperature with the basic detection voltage; and

a flipflop generating the level of the temperature detecting signal according to results of the comparisons from said first and second differential amplifiers.

5. The semiconductor integrated circuit according to claim 2, further comprising:

a voltage generator generating a plurality of kinds of voltages;

a switch circuit selecting two kinds from the plurality of kinds of voltages to output the selected two as a first and a second reference voltage; and

a ROM circuit presetting voltages to be selected by said switch circuit.

6. The semiconductor integrated circuit according to claim 1, further comprising

a memory array having dynamic memory cells, wherein

said control circuit is a refresh timer which changes a generation cycle of a refresh request signal according to the level of the temperature detecting signal, the refresh request

signal being for refreshing the memory cells.

7. The semiconductor integrated circuit according to claim 6, further comprising:

a command decoder decoding a read command signal and a write command signal that are access requests supplied via an external terminal; and

an operation control circuit outputting a timing signal for putting said memory array into operation in order to execute an access operation in response to the read command signal and the write command signal and a refresh operation in response to the refresh request signal, wherein

said operation control circuit has an arbiter determining which one of the access operation and the refresh operation is to be given priority when the read command signal or the write command signal conflicts with the refresh request signal.

8. The semiconductor integrated circuit according to claim 6, further comprising:

a command decoder decoding a read command signal, a write command signal, and a self refresh command signal during a normal operation mode, the read and write command signals being access requests supplied via an external terminal, the self refresh signal being for changing the normal operation mode to a self refresh mode; and

an operation control circuit outputting a timing signal for putting said memory array into operation in order to execute an access operation in response to the read command signal and the write command signal and a refresh operation in response to the refresh request signal, wherein

said refresh timer starts operating when said command decoder decodes the self refresh command signal.